Introduction to Digital Logic

EECS/CSE 31L

**Assignment 1:**

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**1.1 Assignment Description**

Follow the instructions in the tutorial for each tool appended to this text. CAD tools you will work with them in this assignment are:

**Tool 1:** ISE WebPACK design software from Xilinx

**Tool 2:** ModelSim from Mentor Graphics

**Tool 3:** Incisive Enterprise Simulator from Cadence

**1.2 Assignment Deliverable**

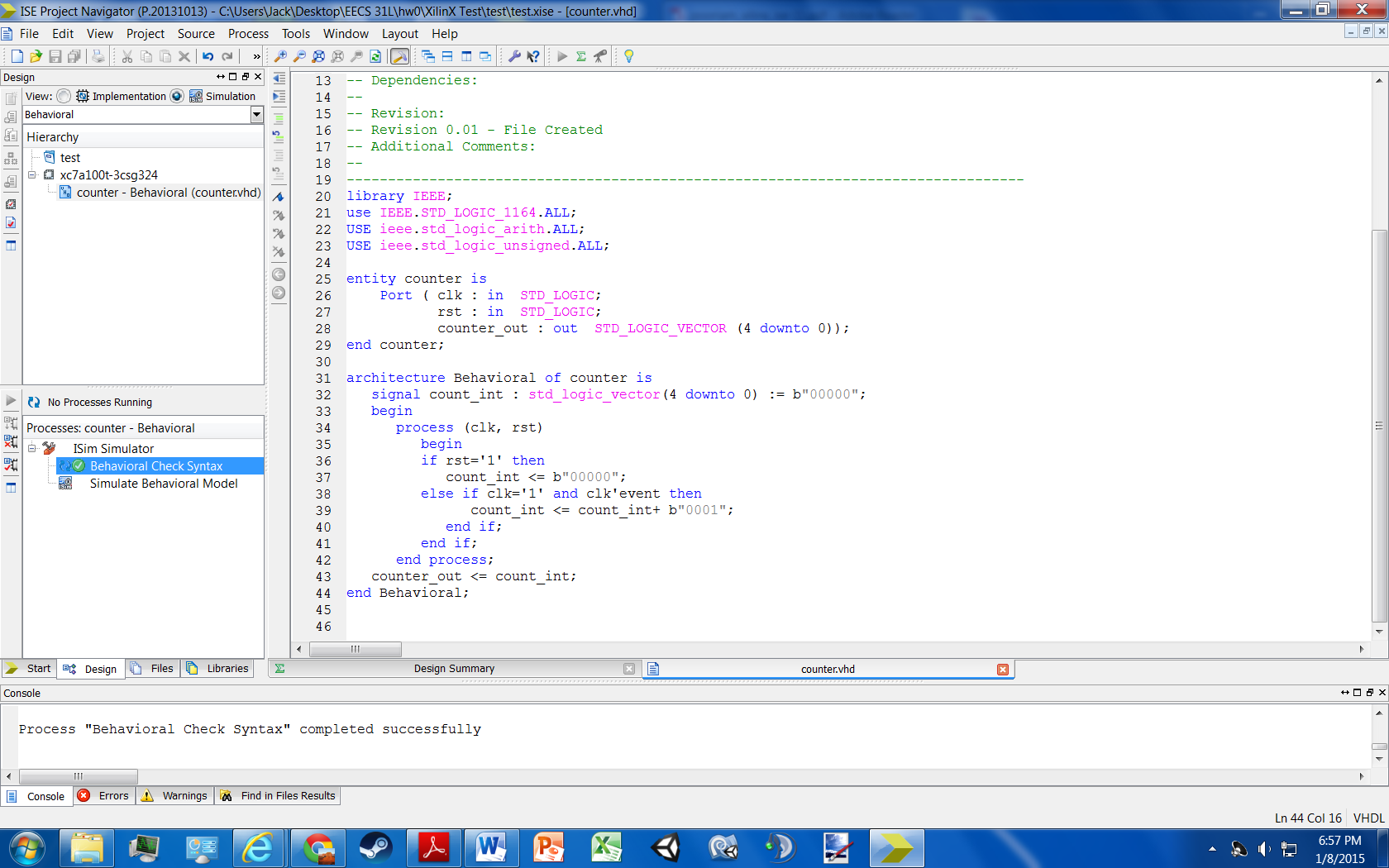
**XilinX ISE**

• A short report on what you have learned

I learned how to:

* create a new project in XilinX
* Create and add new VHDL modules to the project
* Check VHDL file for syntax errors
* Create a new VHDL test bench and check it for syntax errors
* Compile and run a simulation and display a waveform

• Compilation, Elaboration, and Simulation logs



Firgure 1: Check counter.vhd for syntax errors

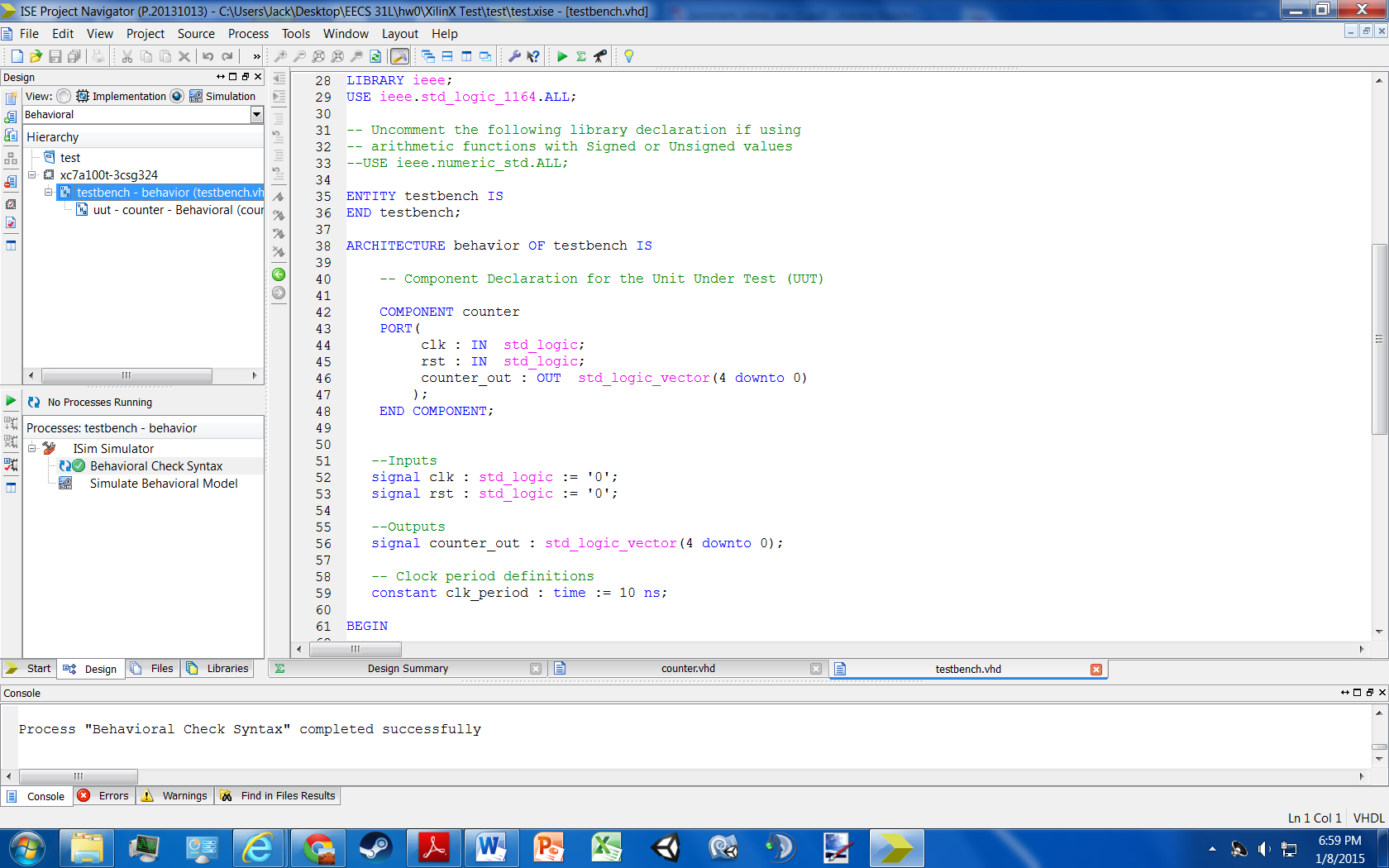


Figure 2: Check testbench.vhd for syntax errors

**XilinX Simulation Log**

Started : "Simulate Behavioral Model".

Determining files marked for global include in the design...

Running fuse...

Command Line: fuse -intstyle ise -incremental -lib secureip -o {C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_isim\_beh.exe} -prj {C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_beh.prj} work.testbench {}

Running: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\fuse.exe -intstyle ise -incremental -lib secureip -o C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_isim\_beh.exe -prj C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_beh.prj work.testbench

ISim P.20131013 (signature 0x7708f090)

Number of CPUs detected in this system: 4

Turning on mult-threading, number of parallel sub-compilation jobs: 8

Determining compilation order of HDL files

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/counter.vhd" into library work

Parsing VHDL file "C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench.vhd" into library work

Starting static elaboration

Completed static elaboration

Compiling package standard

Compiling package std\_logic\_1164

Compiling package std\_logic\_arith

Compiling package std\_logic\_unsigned

Compiling architecture behavioral of entity counter [counter\_default]

Compiling architecture behavior of entity testbench

Time Resolution for simulation is 1ps.

Waiting for 1 sub-compilation(s) to finish...

Compiled 7 VHDL Units

Built simulation executable C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_isim\_beh.exe

Fuse Memory Usage: 34000 KB

Fuse CPU Usage: 514 ms

Launching ISim simulation engine GUI...

"C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "C:/Users/Jack/Desktop/EECS 31L/hw0/XilinX Test/test/testbench\_isim\_beh.wdb"

ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully

• Waveform snapshot from each tool

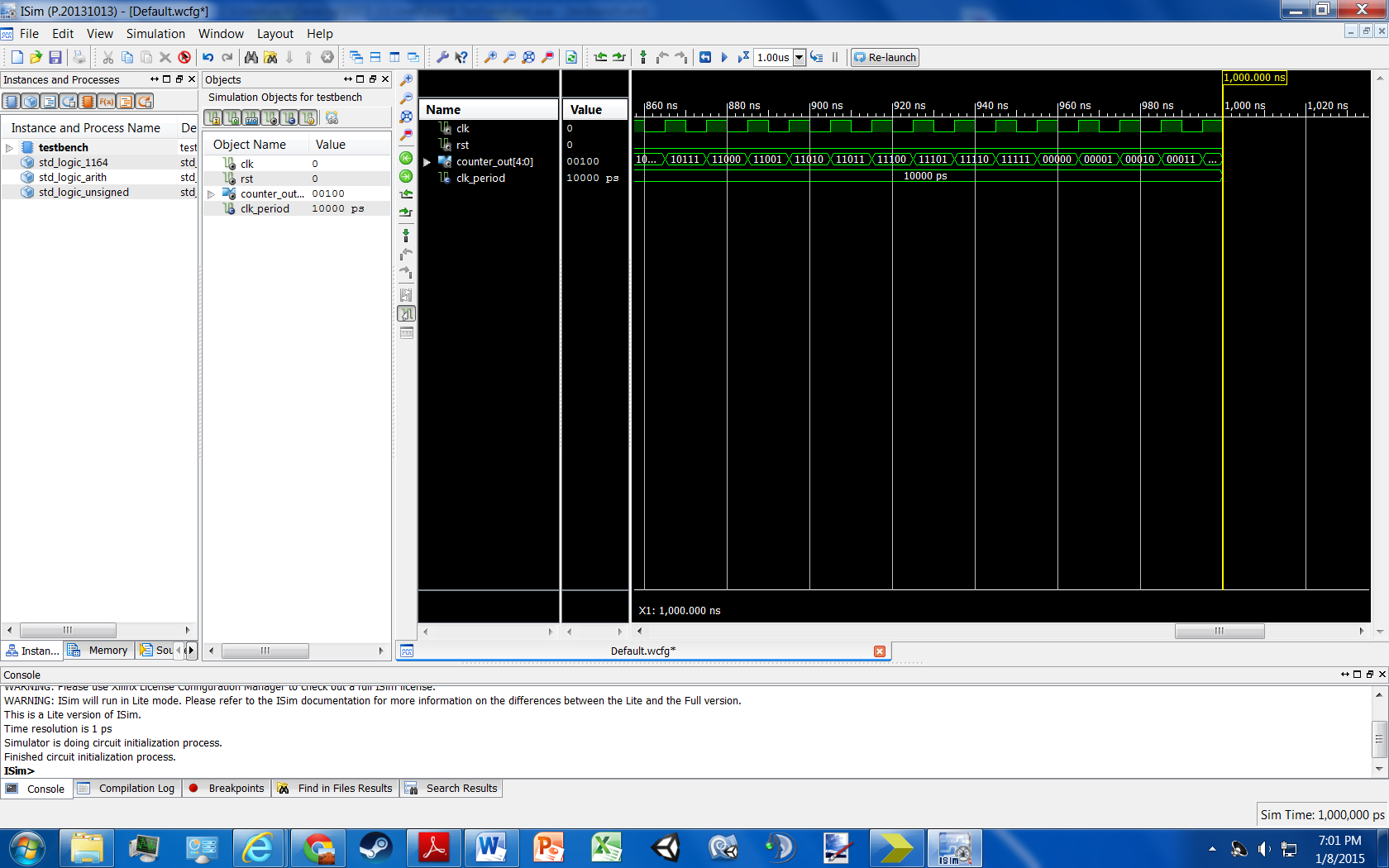


Figure 3: Waveform of counter.vhd simulation

**ModelSim**

• A short report on what you have learned

I learned how to:

* create a new project in ModelSim
* Create and add new files to the project
* Compile a VHDL file
* Setup a simulation
* Adjust how long the simulation is run for
* Setup clocks for the input values or change them manually
* Run a simulation to acquire a waveform and simulation logs

• Compilation, Elaboration, and Simulation logs

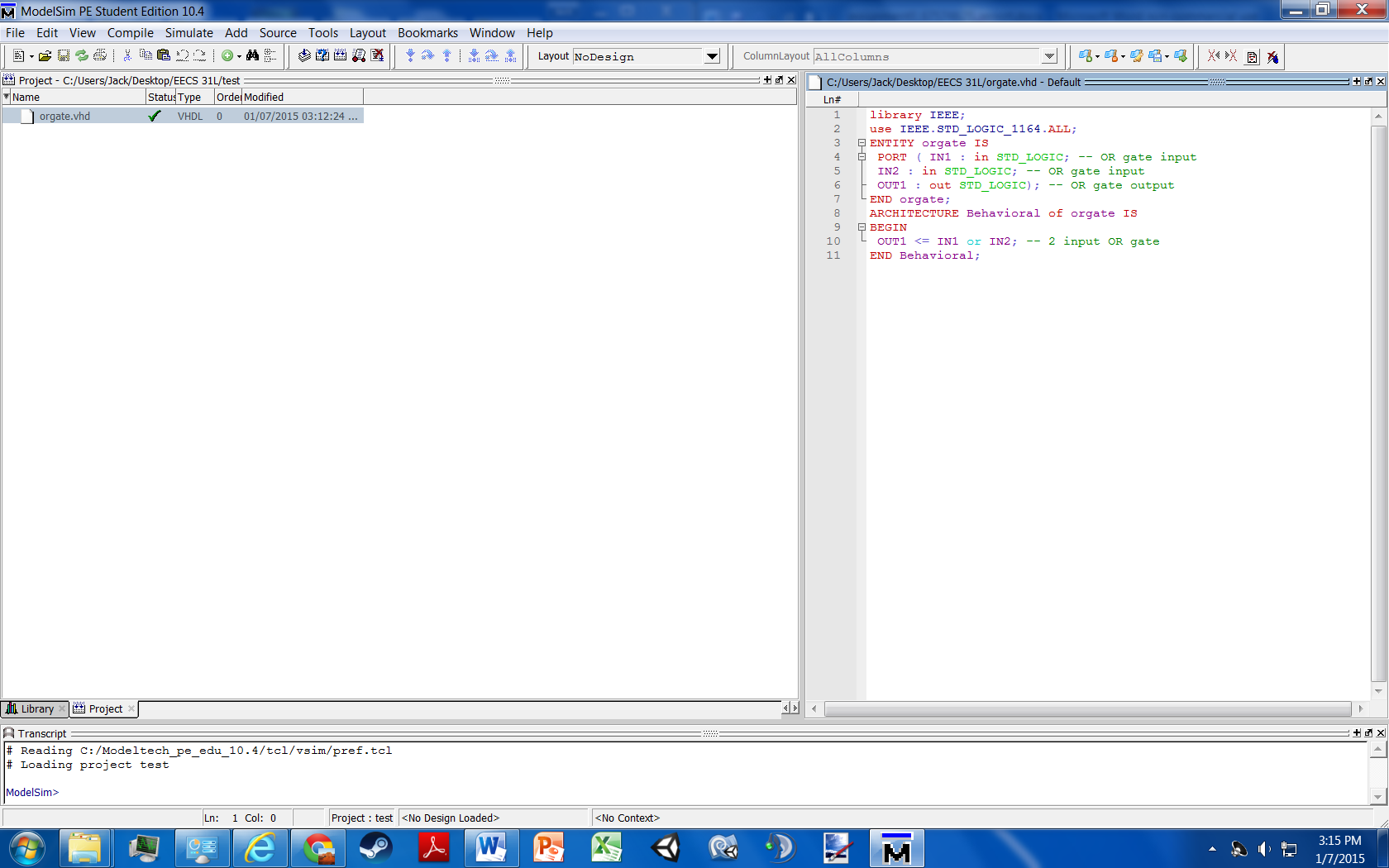


Figure 4: Compile orgate.vhd

**ModelSim Simulation Log**

force –freeze sim:/orgate/IN1 1 0, 0 {50 ns} –r 100

force –freeze sim:/orgate/IN2 1 0, 0 {100 ns} –r 200

VSIM 9> run

VSIM 10> quit –sim

• Waveform snapshot from each tool

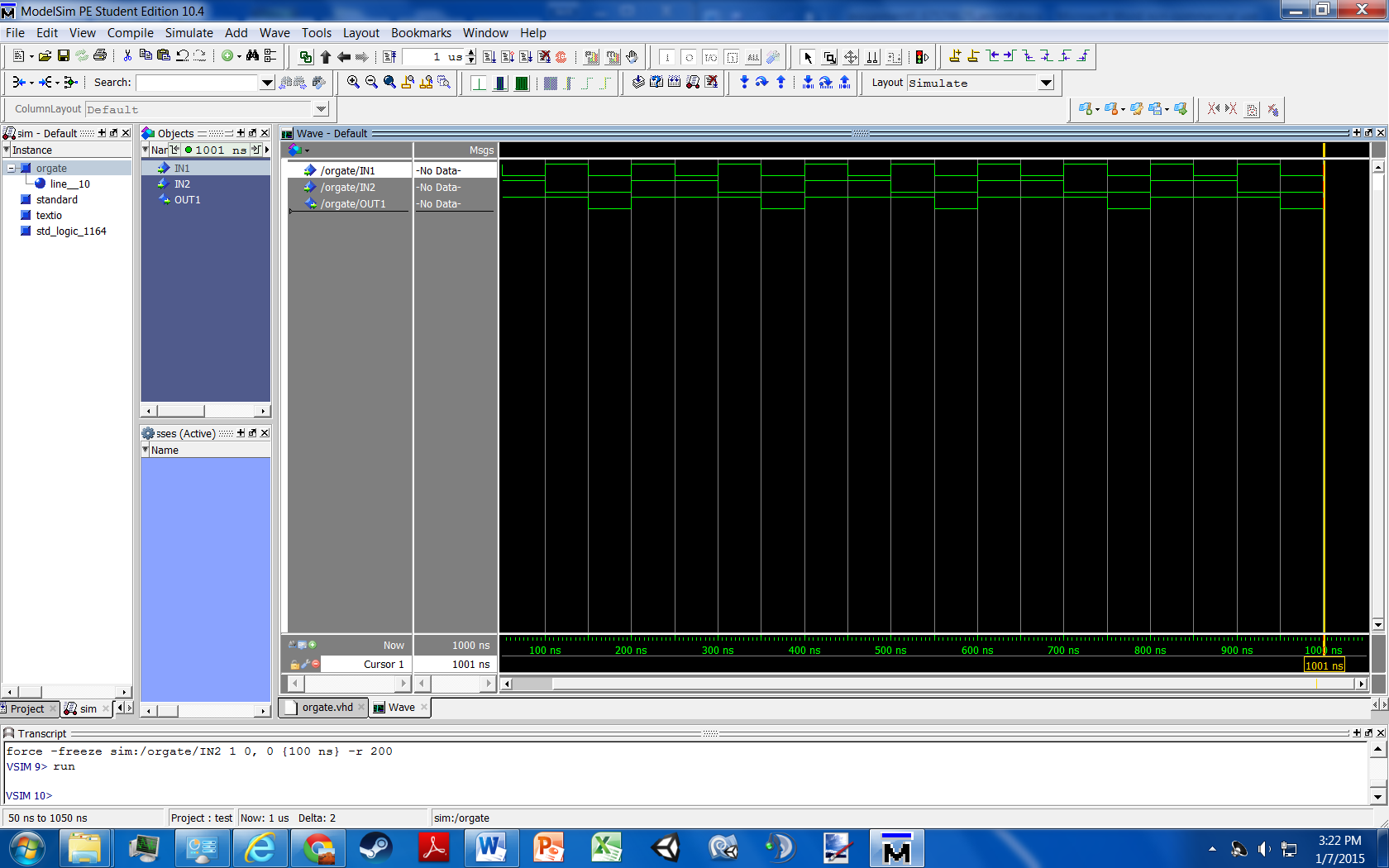


Figure 6: Waveform of orgate simulation